An All - Digital Frequency Locked Loop (ADFLL) with a Pulse Output Direct Digital Frequency Synthesizer (DDFS) and an Adaptive Phase Estimator

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Abstract — **An algorithm for frequency synthesizing all-digital frequency locked loops (ADFLLs) with fast frequency acquisition is presented in this paper. A Pulse Output Direct Digital Frequency Synthesizer (DDFS) with reduced hardware cost and architecture, full digitization, easy design and implementation is proposed. An adaptive phase estimator is also proposed. The DDFS has 16-bit binary weighted control and the simulations show that the ADFLL can operate in the frequency range between 50 MHz and 500 MHz.**

Index Terms – All-digital Phase Locked Loops (ADPLLs), frequency synthesizer, phase locked loop.

I. Introduction

The Phase Locked Loops (PLLs) are widely used in modern communication systems and high performance microprocessors because of their remarkable versatility. A PLL may be used to generate an output signal whose frequency is a programmable, rational multiple of a fixed input frequency. PLLs may also be used to perform frequency modulation, demodulation as well as to regenerate the carrier from an input signal in which the carrier has been suppressed [1]. Digital designs can easily fit in the baseband designs and therefore they are widely used in many modern applications such as digital signal processing, microprocessors, clock recovery and generation of clock signals [2]. It is also possible to achieve fast lock times using Digital PLLs. PLLs are used to lock or track input signals in phase and frequency. In communication applications, PLLs are used to make local clocks synchronous with other signals. Therefore it is important to lock the signals in both phase and frequency.

This paper describes a Frequency Synthesizing All Digital Frequency Locked Loop (ADFLL) together with an Adaptive Phase Estimator. The ADFLL is composed of the Frequency Estimator, Control Logic, and the Direct Digital Frequency Synthesizer (DDFS). The Frequency Estimator uses a binary search algorithm to capture the required frequency. The DDFS has 16 bit of binary weighted control and an operating frequency range between 50 MHz and 500 MHz.

The rest of the paper is organized as follows. The proposed architecture and lock mechanism of the ADFLL are described in Section II. Section III presents the circuits design of the ADFLL. Implementation and simulation results are discussed in Section IV.

II. Architecture and Lock Mechanism of the ADFLL

Fig. 1 depicts the block diagram of the ADFLL. The Frequency Estimator compares the frequencies of the reference signal, REF_CLK and the most significant bit (MSB) output of the DDFS, MSB_DDFS respectively. The Frequency Estimator uses a binary search algorithm to sweep the frequency of the DDFS in order to match it with the reference clock. It asserts one of the two signals "UP" or "DOWN" after each frequency comparison. The Control Logic changes the Frequency Tuning Word (FTW) based on the output of the Frequency Estimator.

The Pulse Output DDFS forms the core of the ADFLL. The output frequency of the DDFS depends on the input frequency tuning word and the system clock, f_{clk}. When the frequencies are the same, the control logic asserts the FLOCK signal and frequency acquisition is completed.

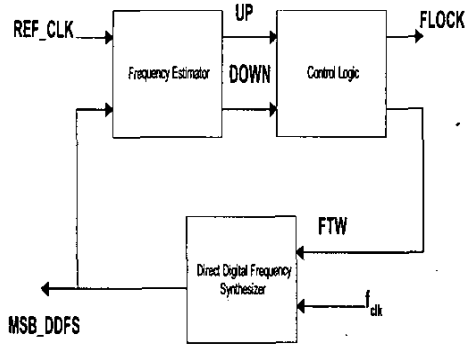

Fig. 1. Block Diagram of the ADFLL

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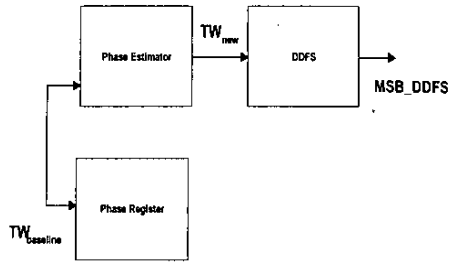

Fig. 2. ADPLL with proposed Phase Estimator

Fig. 2. shows the block diagram of the All Digital Phase Locked Loop (ADPLL) with the proposed Phase Estimator. The Phase Estimator works as follows. Since the frequency is the derivative of phase, a change in frequency will change the phase. Once frequency acquisition is complete, the frequency tuning word, $TW_{baseline}$ is stored in a Phase Register. The Phase Estimator changes the frequency tuning word to TW_{new} to align the phases of the reference and the output signals. Once phase acquisition is complete, the frequency tuning word can be restored to its baseline value, $TW_{baseline}$.

III. Circuits Design of ADFLL

A. Pulse Output DDFS

The Pulse Output Direct Digital Frequency Synthesizer is the simplest type of a Direct Digital Frequency Synthesizer (DDFS) [3]. The output of a DDFS represents the instantaneous amplitude of the signal. The task of the DDFS is therefore to generate this sinusoid oscillating number. For a constant frequency ω, the phase $d\phi/dt$ is also a constant. The phase change of a constant frequency is a linear progression. Therefore a digital phase accumulator can be used to integrate the frequency to provide the digital phase information. Fig. 3 represents the block diagram of this type of DDFS. It consists of a FTW Register in conjunction with an N–bit Phase Accumulator driven by system clock, f_{clk}. The frequency register holds the n– bit FTW. For each clock cycle, the frequency is added to the phase accumulator. The lowest frequency that can be generated occurs when just 1 LSB (least significant bit) is added to the accumulator. Thus the phase accumulator increments every time through all possible states until it overflows. This takes 2^N clock cycles for an N bit accumulator thus the output frequency is $f_{clk}/2^N$. Thus the addition of the number FTW to the accumulator for each cycle of the clock results in the output frequency of FTW * $f_{clk}/2^N$. Thus (1) gives the output frequency of the Pulse Output DDFS.

$$f_{out} = \frac{FTW * f_{clk}}{2^N} \qquad \ldots\ldots (1)$$

For the Pulse Output DDFS, the MSB or the carry output of the phase accumulator is used as the output. The sine wave oscillation can be visualized as a vector rotating around a phase wheel as shown in Fig. 4 [4]. Each point on the wheel corresponds to an equivalent point on the sine waveform. Thus as the phase accumulator increments through all the possible states, it results in the completion of one cycle of the sine waveform. The number of discrete points on the wheel is determined by the resolution, N of the accumulator.

The phase accumulator provides the vector's linear representation around the phase wheel. Fig. 5. shows the phase accumulator output.

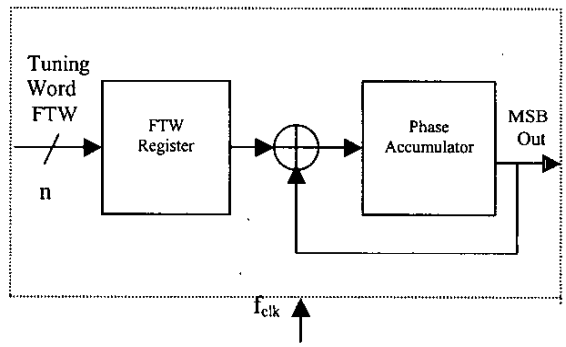

Fig. 3. Block Diagram of a Pulse Output DDFS

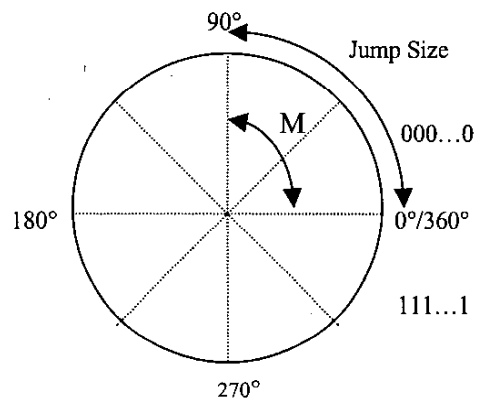

Fig. 4. Phase Wheel Representation

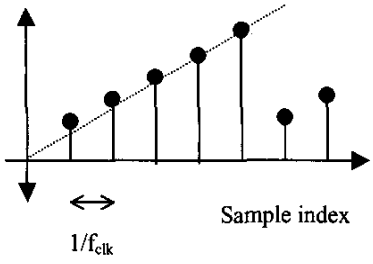

Fig. 5. Phase Accumulator Output

B. *Frequency Estimator and Control Logic*

The Frequency Estimator compares the reference or the input clock and the output of the DDFS. Fig. 6 shows the block diagram of the Frequency Estimator.

A binary search algorithm is used to sweep the frequency of the DDFS in progressively smaller increments [5]. The algorithm begins by initializing the FTW Register, Add Gain and Subtract Gain Registers. The frequency estimator generates signals "UP" or "DOWN" based on the comparison. If the output frequency is less than that of the reference signal, the Frequency Estimator generates a "UP" signal. Otherwise, a "DOWN" signal is generated. The Control Logic changes the FTW register by either adding to or subtracting from it the contents of the gain registers. If a change in search direction occurs, the control logic changes the contents of the frequency gain registers. After every comparison, the Control Logic also provides the FTW to the DDFS. The algorithm proceeds iteratively with successive frequency comparisons until the control logic asserts the "FLOCK" signal.

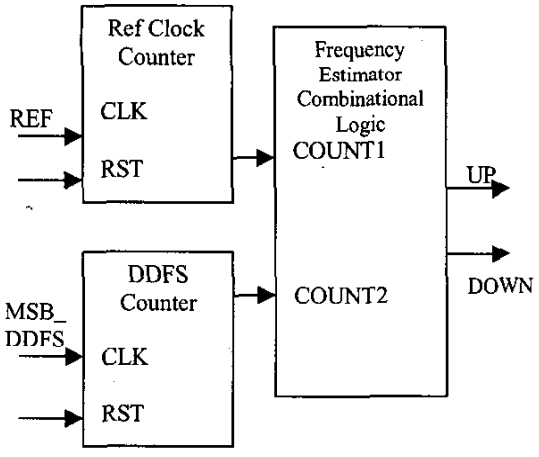

Fig. 6. Block Diagram of the Frequency Estimator

IV. Implementation and Simulation Results

All the parts of the ADFLL were designed using Verilog HDL. The ADFLL was designed with Verilog HDL and the standard cell library CMOS 0.5-micron process. The ADFLL runs up to 500 MHz. Fig. 7 shows the Chip Layout of the proposed ADFLL. Fig. 8 shows the post layout simulation results using Cadence SPECTRE tools. The simulation results illustrate the frequency lock phenomena.

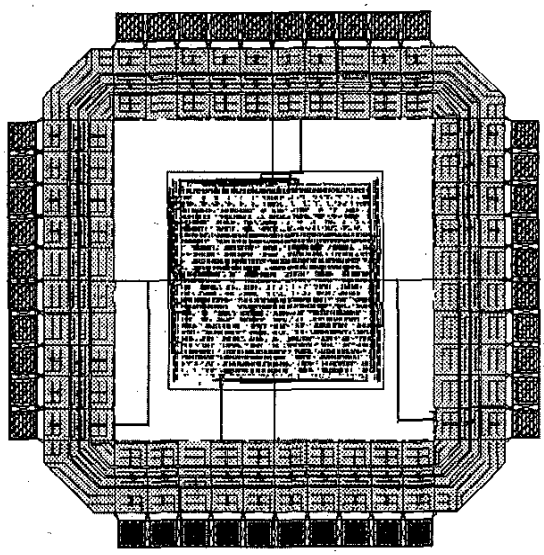

Fig. 7. Chip Layout of the proposed ADFLL

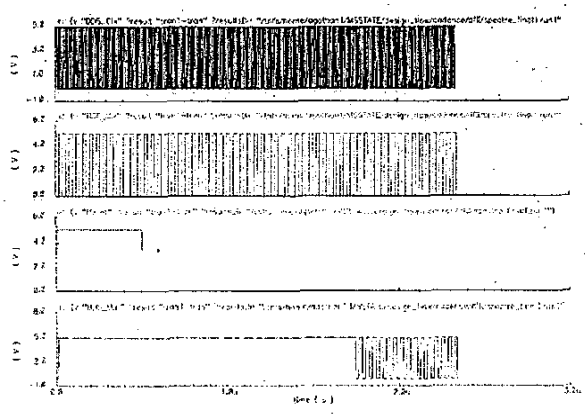

Fig. 8. Post Layout Simulation Results, REF_CLK = 25 MHz and f_{clk} = 100 MHz

V. Conclusion

An ADFLL circuit and an adaptive phase estimator is proposed in this paper. The Pulse Output DDFS has the characteristics of simplicity and reduced hardware cost. A binary search algorithm is used to achieve fast frequency locking. The post layout simulation results show that the circuit can operate in the frequency range of 50 MHz to 500 MHz. A prototype of the design is being fabricated for performance verification using a 0.5-micron CMOS process from MOSIS.

Acknowledgement

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